Remarks/Arguments:

Reconsideration of the application is requested.

Claims 1-31 remain in the application.

In the third paragraph on page 2 of the above-identified Office action, claims 1-31 have been rejected as fully anticipated by Rajeevakumar (U.S. Patent No. 5,658,816) under 35 U.S.C. § 102.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references.

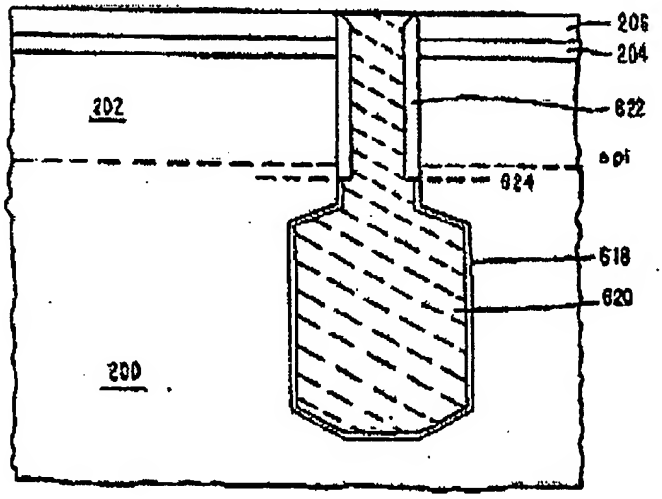
Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, *inter alia*:

doping surfaces of the lower trench regions with a material of a second conductivity type resulting in first electrodes being produced on surfaces of the lower trench regions.

The Rajeevakumar reference discloses the manufacturing of a storage trench of a DRAM cell on a "doped silicon substrate 200 with a lightly doped epitaxial layer 202 of silicon" (column 2, lines 54-55). The trench has a capacitor dielectric (618), a polysilicon fill (620) and an insulating collar (622) (Fig. 6, provided below)

FIG. 6



The reference does not show **doping** surfaces of the lower trench regions with a material of a **second** conductivity type resulting in first electrodes being produced on surfaces of the lower trench regions, as recited in claim 1 of the instant application. The Rajeevakumar reference discloses the

manufacturing of a storage trench of a DRAM cell on a doped silicon substrate with a lightly doped epitaxial layer of silicon. The trench has a capacitor dielectric, a polysilicon fill and an insulating collar. Rajeevakumar **does not** disclose a **doping** of the surfaces of the lower trench regions. In particular, Rajeevakumar **does not** disclose doping of the lower trench regions with a material of a **second** conduction type. This is contrary to the invention of the instant application as claimed, which recites **doping** surfaces of the lower trench regions with a material of a **second** conductivity type resulting in first electrodes being produced on surfaces of the lower trench regions

Since claim 1 is believed to be allowable over Rajeevakumar, dependent claims 2-31 are believed to be allowable over Rajeevakumar as well.

Even though claim 1 is believed to be allowable, the following remarks pertain to the non-obviousness of claim 1.

The Rajeevakumar reference **does not** show or suggest doping surfaces of the lower trench regions with a material of a **second** conductivity type. This feature of the present invention ensures that since, according to claim 1, the substrate is of a first conductivity type, a pn-junction is

provided along the first electrode for electrically insulating the first electrode from the circuit elements (e.g. the selection transistor) on the surface of the semiconductor substrate (page 26, lines 11-15). The present invention discloses that in order to obtain a higher level of memory cell integration, electrical insulation between the circuit elements and the first electrode is an important issue because it represents a "problem zone" that may lead to an undesired short circuit (page 3, line 21, to page 4, line 9 of the specification).

The Rajeevakumar reference starts out with a different material having a "doped silicon substrate (200) with a lightly doped epitaxial layer (202) of silicon." A memory cell based on this material, does not envisage the use of a first electrode having a conductivity type opposite to the substrate since the insulation between first electrode and circuit element is obtained by the lightly doped epitaxial layer (202).

Accordingly, Rajeevakumar does not disclose anything pertaining to the issue of electrically insulating the capacitor from the electric circuit. In particular, Rajeevakumar does not disclose anything pertaining to the

issue of providing the first electrode with a conductivity type opposite to the substrate.

Therefore, Rajeevakumar does provide a person of ordinary skill in the art with any motivation to provide for a first electrode having a conductivity type opposite to the substrate's conductivity type. Accordingly, Rajeevakumar does not provide a person of ordinary skill in the art with any motivation to carry out a step of doping of the lower trench regions with a material of a second conduction type, as recited in claim 1 of the instant application.

Therefore, claim 1 is not obvious over the Rajeevakumar reference.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-31 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel respectfully requests a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner & Greenberg P.A., No. 12-1099.

Respectfully submitted,

For Applicant(s)

Alfred K. Dassler
52,794

AKD:cgm

September 23, 2005

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101